

WHAT IS CLAIMED IS:

1. A double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

5 a transmit circuit, responsive to the clock signal, to sample serial transmit data on the clock rising edge to generate a first transmit serial stream, the transmit circuit, responsive to the clock signal, to sample the serial transmit data on the clock falling edge to generate a second transmit
10 serial stream;

a receive circuit, responsive to the clock signal, to generate a receive serial stream from two receive data streams, the receive serial stream having a first operating frequency, each of the two receive data streams having a
15 second operating frequency, the first operating frequency being about twice the second operating frequency;

a transmit port corresponding to the transmit circuit, including a single pin to communicate the serial transmit data to the transmit circuit; and

20 a receive port corresponding to the receive circuit, including a single pin to communicate the receive serial stream from the receive circuit.

2. The double data rate SMII circuit of Claim 1 wherein the interface circuit is included in a PHY transceiver.

3. The double data rate SMII circuit of Claim 1 wherein the transmit circuit includes a plurality of transmit circuits, each of the transmit circuits having a corresponding port that includes a single pin.

4. The double data rate SMII circuit of Claim 1 wherein the receive circuit includes a plurality of receive circuits, each of the receive circuits having a corresponding port that includes a single pin.

5. The double data rate SMII circuit of Claim 3 wherein the clock signal is derived from a single clock; and

each of the plurality of transmit circuits is responsive to the clock signal.

6. The double data rate SMII circuit of Claim 5 wherein the serial transmit data has a first operating frequency and each of the first transmit serial stream and the second transmit serial stream have a second operating frequency, the first operating frequency being about twice the second operating frequency.

7. The double data rate SMII circuit of Claim 6 wherein the serial transmit data first operating frequency is about equal to the receive serial stream first operating frequency.

8. A PHY transceiver, comprising:

a double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

a transmit circuit, responsive to the clock signal, to sample serial transmit data on the clock rising edge to generate a first transmit serial stream, the transmit circuit, responsive to the clock signal, to sample the serial transmit data on the clock falling edge to generate a second transmit serial stream;

a receive circuit, responsive to the clock signal, to generate a receive serial stream from two receive data streams, the receive serial stream having a first operating frequency, each of the two receive data streams having a second operating frequency, the first operating frequency being about twice the second operating frequency;

a transmit port corresponding to the transmit circuit, including a single pin to communicate the serial transmit data to the transmit circuit; and

a receive port corresponding to the receive circuit, including a single pin to communicate the receive serial stream from the receive circuit.

9. The PHY transceiver of Claim 8 wherein the transmit circuit includes a plurality of transmit circuits, each of the transmit circuits having a corresponding port that includes a single pin; and

wherein the receive circuit includes a plurality of receive circuits, each of the receive circuits having a corresponding port that includes a single pin.

10. The PHY transceiver of Claim 9 wherein the clock signal is derived from a single clock; and

each of the plurality of transmit circuits is responsive to the clock signal.

11. The PHY transceiver of Claim 10 wherein the serial transmit data has a first operating frequency and each of the first transmit serial stream and the second transmit serial

stream have a second operating frequency, the first operating frequency being about twice the second operating frequency.

12. The PHY transceiver of Claim 11 wherein the serial transmit data first operating frequency is about equal to the receive serial stream first operating frequency.

13. A double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

first means for sampling serial transmit data on the clock signal rising edge such that a first transmit serial stream is generated;

second means for sampling the serial transmit data on the clock signal falling edge such that a second transmit serial stream is generated;

means for generating a receive serial stream from two receive data streams, the receive serial stream having a first operating frequency, each of the two receive data streams having a second operating frequency, the first operating frequency being about twice the second operating frequency;

first means for communicating the serial transmit data, including a single pin; and

second means for communicating the receive serial stream from the means for generating, including a single pin to communicate.

14. The double data rate SMII circuit of Claim 13 wherein the interface circuit is included in a PHY transceiver.

15. The double data rate SMII circuit of Claim 13 wherein the first and second sampling means include a plurality of first and second sampling means, each of the plurality of first and second sampling means to sample corresponding serial transmit data having a corresponding port that includes a single pin.

16. The double data rate SMII circuit of Claim 13 wherein the means for generating includes a plurality of generating means, each of the plurality of generating means having a corresponding port that includes a single pin.

17. The double data rate SMII circuit of Claim 15 wherein the clock signal is derived from a single clock; and each of the plurality of the first and second sampling means is responsive to the clock signal.

19. The double data rate SMII circuit of Claim 18 wherein the serial transmit data first operating frequency is about equal to the receive serial stream first operating frequency.

20. A PHY transceiver, comprising:

a double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

first means for sampling serial transmit data on the clock signal rising edge such that a first transmit serial stream is generated;

second means for sampling the serial transmit data on the clock signal falling edge such that a second transmit serial stream is generated;

second means for communicating the receive serial stream from the means for generating, including a single pin to communicate.

wherein the means for generating includes a plurality of generating means, each of the plurality of generating means having a corresponding port that includes a single pin.

19

each of the plurality of the first and second sampling means is responsive to the clock signal.

23. The PHY transceiver of Claim 22 wherein the serial transmit data has a first operating frequency and each of the first transmit serial stream and the second transmit serial stream have a second operating frequency, the first operating frequency being about twice the second operating frequency.

24. The PHY transceiver of Claim 23 wherein the serial transmit data first operating frequency is about equal to the receive serial stream first operating frequency.

25. A method of communicating data over a double data rate SMII circuit, comprising:

receiving serial transmit data having a first operating frequency;

generating two transmit serial streams as a function of the serial transmit data, each of the transmit serial streams having a second operating frequency that is about one-half the first operating frequency;

receiving two receive serial streams;

generating a receive serial stream from the two receive data streams, the receive serial stream having a first

26. The method of Claim 25 wherein generating the two transmit serial streams includes sampling the serial transmit data on a rising edge of a first clock signal to generate a first of the two transmit serial streams.

27. The method of Claim 26 wherein generating the two transmit serial streams includes sampling the serial transmit data on a falling edge of the first clock signal to generate a second of the two transmit serial streams.

28. The method of Claim 25 wherein generating the receive serial stream includes;

latching a first one of the two receive data streams synchronous with a second clock signal such that a latched output is generated; and

combining the latched output with a second one of the two receive data streams.

29. A double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

5 a receive circuit, responsive to the clock signal, to sample serial transmit data on the clock rising edge to generate a first receive serial stream, the receive circuit, responsive to the clock signal, to sample the serial receive data on the clock falling edge to generate a second receive serial stream;

10 a transmit circuit, responsive to the clock signal, to generate a transmit serial stream from two transmit data streams, the transmit serial stream having a first operating frequency, each of the two transmit data streams having a second operating frequency, the first operating frequency
15 being about twice the second operating frequency;

a transmit port corresponding to the transmit circuit, including a single pin to communicate the serial transmit data from the transmit circuit; and

20 a receive port corresponding to the receive circuit, including a single pin to communicate the receive serial stream to the receive circuit.

30. The double data rate SMII circuit of Claim 29 wherein the interface circuit is included in a MAC.

31. The double data rate SMII circuit of Claim 29 wherein the receive circuit includes a plurality of receive circuits, each of the receive circuits having a corresponding port that includes a single pin.

32. The double data rate SMII circuit of Claim 29 wherein the transmit circuit includes a plurality of transmit circuits, each of the transmit circuits having a corresponding port that includes a single pin.

33. The double data rate SMII circuit of Claim 31 wherein the clock signal is derived from a single clock; and each of the plurality of receive circuits is responsive to the clock signal.

34. The double data rate SMII circuit of Claim 33 wherein the serial receive data has a first operating frequency and each of the first receive serial stream and the second transmit serial stream have a second operating frequency, the first operating frequency being about twice the second operating frequency.

35. The double data rate SMII circuit of Claim 34 wherein the serial receive data first operating frequency is about equal to the receive serial stream first operating frequency.

36. A media access controller, comprising:

a double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

a receive circuit, responsive to the clock signal, to sample serial transmit data on the clock rising edge to generate a first receive serial stream, the receive circuit, responsive to the clock signal, to sample the serial receive data on the clock falling edge to generate a second receive serial stream;

a transmit circuit, responsive to the clock signal, to generate a transmit serial stream from two transmit data streams, the transmit serial stream having a first operating frequency, each of the two transmit data streams having a second operating frequency, the first operating frequency being about twice the second operating frequency;

a transmit port corresponding to the transmit circuit, including a single pin to communicate the serial transmit data from the transmit circuit; and

5 a receive port corresponding to the receive circuit, including a single pin to communicate the receive serial stream to the receive circuit.

37. The media access controller of Claim 36 wherein the receive circuit includes a plurality of receive circuits, each of the receive circuits having a corresponding port that includes a single pin; and

wherein the transmit circuit includes a plurality of transmit circuits, each of the transmit circuits having a corresponding port that includes a single pin.

38. The media access controller of Claim 37 wherein the clock signal is derived from a single clock; and

each of the plurality of receive circuits is responsive to the clock signal.

39. The media access controller of Claim 38 wherein the serial receive data has a first operating frequency and each of the first receive serial stream and the second receive

Atorney Docket No.: MP122
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40. The media access controller of Claim 39 wherein the

41. A double data rate SMII circuit to communicate data

first means for sampling serial receive data on the clock

second means for sampling the serial receive data on the

means for generating a transmit serial stream from two

first means for communicating the serial receive data,
including a single pin; and

second means for communicating the transmit serial stream
from the means for generating, including a single pin to
communicate.

42. The double data rate SMII circuit of Claim 41
wherein the interface circuit is included in a media access
controller.

43. The double data rate SMII circuit of Claim 41
wherein the first and second sampling means include a
plurality of first and second sampling means, each of the
plurality of first and second sampling means to sample
corresponding serial receive data having a corresponding port
that includes a single pin.

44. The double data rate SMII circuit of Claim 41
wherein the means for generating includes a plurality of
generating means, each of the plurality of generating means
having a corresponding port that includes a single pin.

45. The double data rate SMII circuit of Claim 43
wherein the clock signal is derived from a single clock; and

each of the plurality of the first and second sampling means is responsive to the clock signal.

46. The double data rate SMII circuit of Claim 41 wherein the serial receive data has a first operating frequency and each of the first receive serial stream and the second receive serial stream have a second operating frequency, the first operating frequency being about twice the second operating frequency.

47. The double data rate SMII circuit of Claim 46 wherein the serial receive data first operating frequency is about equal to the transmit serial stream first operating frequency.

48. A media access controller, comprising:
a double data rate SMII circuit to communicate data synchronous with a clock signal having a rising edge and a falling edge, comprising:

first means for sampling serial receive data on the clock signal rising edge such that a first receive serial stream is generated;

second means for sampling the serial receive data on the clock signal falling edge such that a second receive serial stream is generated;

means for generating a transmit serial stream from two transmit data streams, the transmit serial stream having a first operating frequency, each of the two transmit data streams having a second operating frequency, the first operating frequency being about twice the second operating frequency;

first means for communicating the serial receive data, including a single pin; and

second means for communicating the transmit serial stream from the means for generating, including a single pin.

49. The media access controller of Claim 48 wherein the first and second sampling means include a plurality of first and second sampling means, each of the plurality of first and second sampling means to sample corresponding serial receive data having a corresponding port that includes a single pin; and

wherein the means for generating includes a plurality of generating means, each of the plurality of generating means having a corresponding port that includes a single pin.

having a second operating frequency that is about one-half the first operating frequency;

receiving two transmit serial streams;

generating a transmit serial stream from the two transmit data streams, the transmit serial stream having a first operating frequency, each of the two transmit data streams having a second operating frequency, the first operating frequency being about twice the second operating frequency.

54. The method of Claim 53 wherein generating the two receive serial streams includes sampling the serial receive data on a rising edge of a first clock signal to generate a first of the two receive serial streams.

55. The method of Claim 54 wherein generating the two receive serial streams includes sampling the serial receive data on a falling edge of the first clock signal to generate a second of the two receive serial streams.

56. The method of Claim 53 wherein generating the transmit serial stream includes;

latching a first one of the two transmit data streams synchronous with a second clock signal such that a latched output is generated; and

combining the latched output with a second one of the two transmit data streams.

57. A network interface circuit to communicate information between at least two Ethernet network ports and a computer, comprising:

a double data rate serial media independent interface, including;

a physical layer component to provide connectivity to the at least two Ethernet network ports, the physical layer component including two interface pins corresponding to each pair of the at least two Ethernet network ports;

a media access control layer component including two interface pins corresponding to each pair of the at least two Ethernet network ports, to communicate uni-directional information with the physical layer component;

the physical layer component and the media access control layer component to communicate the uni-directional information therebetween through the media access control layer component interface pins and the physical layer component interface pins at a double data rate.

58. The network interface circuit of Claim 57 wherein the media access control layer component interface pins include transmit pins and receive pins;

wherein the physical layer component interface pins include transmit pins and receive pins; and

the uni-directional information includes transmit information and receive information.

59. The network interface circuit of Claim 58 wherein the transmit information associated with each pair of ports is interleaved and transmitted through a corresponding single transmit pin included in a one of the physical layer component and the media access control layer component to another corresponding transmit pin included in the other of the physical layer component and the media access control layer component.

60. The network interface circuit of Claim 59 wherein the interleaved transmit information is separated into two streams of transmit information at the other of the physical layer component and the media access control layer component.

61. The network interface circuit of Claim 58 wherein the receive information associated with each pair of ports is interleaved and transmitted through a corresponding single receive pin included in a one of the physical layer component and the media access control layer component to another corresponding receive pin included in the other of the physical layer component and the media access control layer component.

62. The network interface circuit of Claim 61 wherein the interleaved receive information is separated into two streams of receive information at the other of the physical layer component and the media access control layer component.

63. A network interface circuit to communicate information between at least two Ethernet network ports and a computer, comprising:

a double data rate serial media independent interface, including;

means for providing connectivity to the at least two Ethernet network ports, the connectivity means including two interface pins per pair of ports;

the connectivity means and the communicating means to communicate the uni-directional information therebetween through the communicating means interface pin and the connectivity means interface pin at a double data rate.

64. The network interface circuit of Claim 57 wherein the uni-directional information includes transmit information and receive information.

65. The network interface circuit of Claim 58 wherein the transmit information associated with a pair of ports is interleaved and transmitted through a corresponding single transmit pin included in a one of the connectivity means and the communicating means to another corresponding transmit pin included in the other of the connectivity means and the communicating means.

66. The network interface circuit of Claim 59 wherein the interleaved transmit information is separated into two

streams of transmit information at the other of the
connectivity means and the communicating means.

67. The network interface circuit of Claim 58 wherein the receive information associated with a pair of ports is interleaved and transmitted through a corresponding single receive pin included in a one of the connectivity means and the communicating means to another corresponding receive pin included in the other of the connectivity means and the communicating means.

68. The network interface circuit of Claim 61 wherein the interleaved receive information is separated into two streams of receive information at the other of the connectivity means and the communicating means.